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ORIGINAL ARTICLE

# Power quality improvements of arc welding power supplies by modified bridgeless SEPIC PFC converter

**Amar Bouafassa**[1] · **Luis M. Fernández-Ramírez**[2] · **Badreddine Babes**[3]

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**Abstract**
This paper proposes an efficient bridgeless power factor corrected (PFC) modified single ended primary inductor converter (SEPIC) for arc welding power supplies (AWPS). The overall configuration is composed of two converters: (1) a modified bridgeless SEPIC PFC converter, which is controlled by a PI controller to achieve a high power factor and fast response; and (2) a full bridge buck converter with high-frequency transformer for high-frequency isolation to ensure arc welding stability. The proposed system is simulated under different operating conditions of an AWPS. It is also tested in real time by a hardware-in-the-loop system based on a dSPACE DS1103 control board. The system performances are evaluated based on power quality indices such as power factor, total harmonic distortions of the AC grid current, and voltage regulation. The obtained results show that the proposed controller enhances the weld bead quality by keeping a constant current at the output and a stable arc, meet the international power quality standards and robustness for voltage regulation.

**Keywords** Arc welding power supply · Bridgeless PFC converter · Modified single ended primary inductor converter · PI controller

## 1 Introduction

Joining metals have become a fundamental issue in modern industrialized operations. It can be accomplished through different welding processes such as gas welding, resistance welding, arc welding, and so on. Among all these kinds of welding processes, more attention and popularity has been focused on arc welding due to its flexible automation and high efficiency [1, 2].

Due to the excessive heat from electrode wire, important challenges in the development of an arc welding power supply are the control of the feed-rate of the electrode and maintenance of the arc stability since a small arc length variation can induce enormous arc voltage fluctuations that may exceed the maximum allowable range of the power supply. For these reasons, the welding load current must be controlled and limited during overload conditions. The aim of the proposed controller for AWPS is to provide perfect dynamic responses through the regulation of the output voltage and the output current.

A single-phase full bridge buck converter connected at the point of common coupling (PCC) with an uncontrolled diode bridge rectifier has been extensively used for interfacing arc welding power supplies with an AC grid. These have led to several power qualities disturbances at AC mains such as a non-sinusoidal input current and a low power factor. To overcome these drawbacks, active PFC is introduced as a pre-regulator to comply with PQ requirements and international standards such as EN 61000-3-2 and IEEE 519-1992 [3]. PFC converter-based AWPSs have been explored in the literature [4–6]. However, the important requirements of an AWPS have led to the development of power converters suitable for AWPSs such as interleaved canonical switching cell [1], bridgeless boost converter [2], modified zeta converter [4], and canonical switching cell [5].

✉ Amar Bouafassa
amar.bouafassa@gmail.com

[1] Department of Electronics, Electrical Engineering and Automation, National Polytechnic School of Constantine, Constantine, Algeria

[2] Research Group in Sustainable and Renewable Electrical Technologies, Department of Electrical Engineering, Higher Polytechnic School of Algeciras, University of Cadiz, Cadiz, Spain

[3] Research Center in Industrial Technologies (CRTI), Algiers, Algeria

Recently, it has become possible to remove the diode bridge rectifier at the front end of a switched mode power supply either partially or completely. Several bridgeless converter topologies have been reported [7–10]. It has been noticed from existing works that bridgeless converters offer high efficiency with reduced EMI losses, which makes them suitable for the front end of AWPS and other high-power industrial applications.

Due to its simplicity, the most common PFC circuit used in bridgeless topologies is the boost converter.

However, the PFC boost converter suffers from lower efficiency and high voltage stress which degrades the performance of the converter and limits the application range. Moreover, it has practical limitations such as high inrush current and unsatisfactory current handling capability under over load conditions [11]. To overcome these issues, the bridgeless SEPIC converter was introduced in the literature [11–14]. The bridgeless SEPIC converter offers many prominent merits such as limiting inrush current at startup and overloading conditions, reduced stresses to enhance the efficiency, and the ability to meet the challenges of a near unity power factor and output voltage regulation.

Due to the advantages offered by the SEPIC converter such as highly step up/down conversion without inverting the output and support for short-circuit operating conditions, they represent an interesting option to enhance the operating performance of AWPS. When compared to boost or buck converters, classical SEPIC converters include an extra inductor and capacitor, which leads to additional power losses and reduced power conversion efficiency. To solve the aforementioned problems in classical SEPIC and PFC-based AWPS, a bridgeless modified SEPIC PFC converter is introduced in this paper to enhance the AWPS operation and to comply the power quality requirements.

The main goals of the proposed control in this paper are as follows: (i) improving the weld bead quality by restricting the output current to a desired limit, (ii) improving the arc welding performances by regulating the output voltage along with the output current to a desired value during overload conditions, (iii) ensuring good stability in the arc welding process, (iv) achieving a fast response.

The configuration and control scheme for the AWPS are simulated in MATLAB/Simulink, and tested in real time using a HIL system based on a dSPACE DS1103 control board. The obtained results have clearly satisfied the requirements of PQ and follow-up references over a wide range of load and voltage variations, which allows for the realization of a high-quality weld.

## 2 System description

The system under study is depicted in Fig. 1. It is composed of three main blocks. (i) A modified bridgeless SEPIC PFC converter. (ii) A single-phase full-bridge buck converter connected at the point of common coupling with a controlled rectifier. (iii) A high frequency transformer (HFT) for ensuring high galvanic isolation.

### 2.1 Modified bridgeless SEPIC PFC converter

The modified bridgeless SEPIC PFC rectifier is shown in Fig. 2. It has two power switches $S_1$ and $S_2$ that are controlled by the same signal. When the switches $S_1$ and $S_2$ are turned

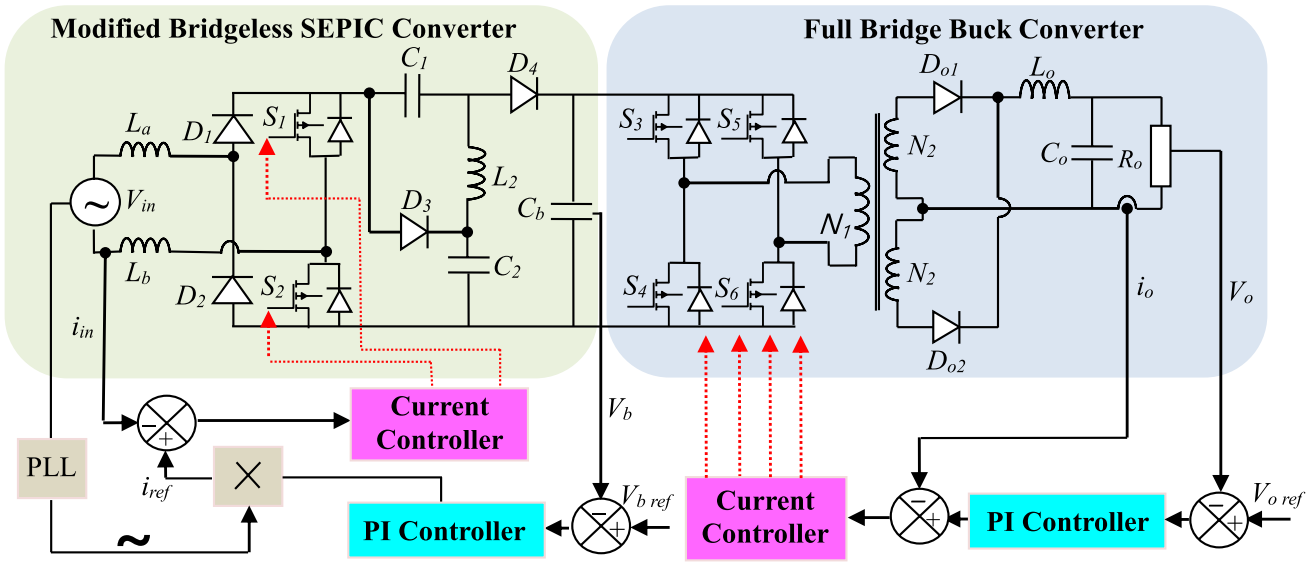


**Fig. 1** Synoptic description of the studied circuit

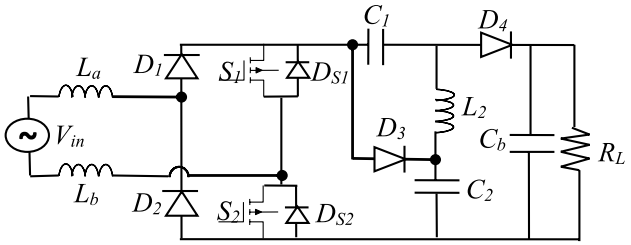


**Fig. 2** Modified bridgeless SEPIC PFC converter [7]

OFF, the energy is transferred to the capacitor $C_1$. When $S_1$ and $S_2$ are turned ON, the energy stored in the capacitor is transferred to the output load. The modified bridgeless SEPIC PFC rectifier topology decreases the conduction losses and voltage stress. Hence, the power conversion efficiency increases [7].

There are three operation modes in the modified bridgeless SEPIC PFC converter [7] as illustrated in Fig. 3. The sum of the inductors $L_a$ and $L_b$ is assumed to be $L_1$ to simplify the circuit analysis. The high power factor of the SEPIC converter is achieved by operating the input inductor $L_1$ in the DCM. Meanwhile, the output inductor $L_0$ operates in the CCM. The input current "$i_{L1}$" is a function of $\sin(\omega_s{*}t)$ and it follows the input voltage $V_{in}{*}\sin(\omega_s{*}t)$. Thus, unity power factor operation is achieved for the modified bridgeless SEPIC PFC converter.

#### 2.1.1 First stage [$t_0$, $t_1$]

During this subinterval, the switches $S_1$ and $S_2$ are turned ON simultaneously as shown in Fig. 3a. The current $i_{L1}$ increases with a slope of $V_{in}/L_1$ and the inductor current $i_{L2}$ decreases with a slope of $-(-V_{C1}+V_{C2})/L_2$ as follows:

$$i_{L1}(t) = i_{fw}(t) + \frac{V_{in}}{L_1}(t - t_0), \tag{1}$$

$$i_{L2}(t) = i_{fw}(t) - \frac{-V_{C1} + V_{C2}}{L_2}(t - t_0), \tag{2}$$

where $i_{fw}$ is the freewheeling current, $V_{L1} = V_{in}$, and $V_{L2} = -(-V_{C1} + V_{C2})$.

From Eqs. (1) and (2), the main switch current $i_{S1}$ is expressed as:

$$i_{S1}(t) = i_{L1}(t) - i_{L2}(t) = \left(\frac{V_{in}}{L_1} + \frac{-V_{C1} + V_{C2}}{L_2}\right)(t - t_0). \tag{3}$$

#### 2.1.2 Second stage 2 [$t_1$, $t_2$]

In this stage, the switches $S_1$ and $S_2$ are turned OFF simultaneously, while the diode $D_3$ turns ON. Hence, the main

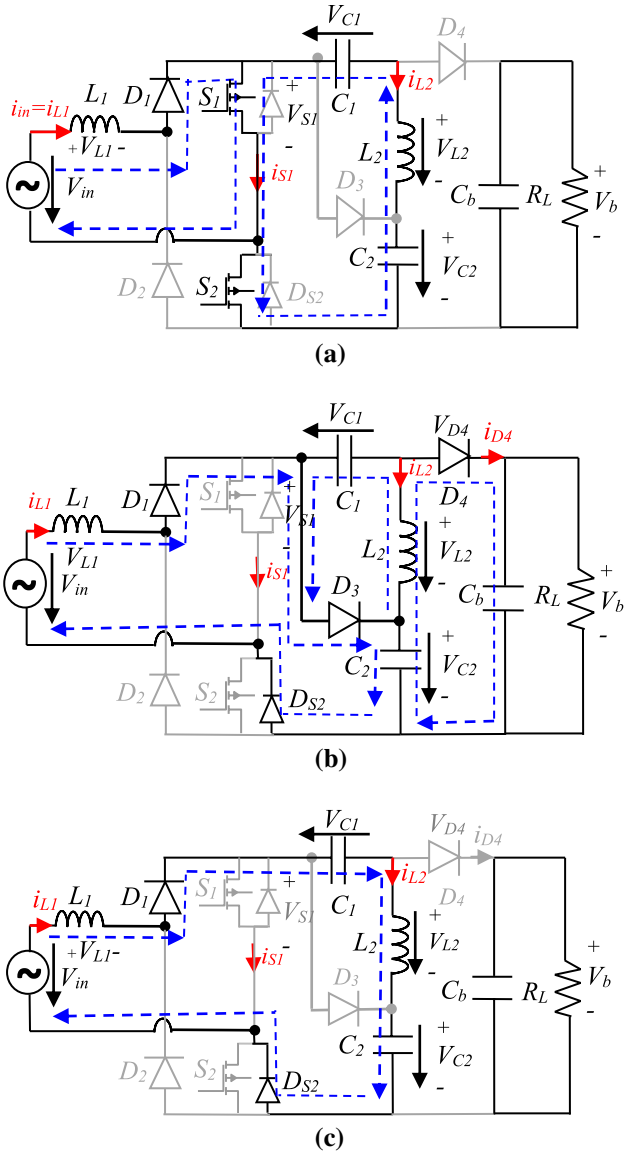


**Fig. 3** Operation modes of the modified bridgeless SEPIC converter: **a** stage 1. **b** stage 2. **c** stage 3 [7]

switch voltage $V_{S1}$ is clamped to $V_{C2}$. The current $i_{L1}$ is decreased from its peak value $i_{L1}(t_1)$ as follows:

$$i_{L1}(t) = i_{L1}(t_1) - \frac{-V_{in} + V_{C2}}{L_1}(t - t_1). \tag{4}$$

The current $i_{L2}$ increases from the bottom value $i_{L2}(t_1)$ according to:

$$i_{L2}(t) = i_{L2}(t_1) + \frac{V_{C1}}{L_2}(t - t_1), \tag{5}$$

where $V_{L2} = V_{C1}$ and $V_{L1} = -(-V_{in} + V_{C2})$.

In this stage, the time ratio $\Delta_1$ is the ratio of the time interval between $t_1$ and $t_2$. It can be calculated as:

$$V_{in}DT_s - (-V_{in} + V_{C2})\Delta_1 T_s = 0, \tag{6}$$

where

$$V_{C2} = \frac{V_b + V_{in}}{2}. \tag{7}$$

From Eqs. (6) and (7), $\Delta_1$ is expressed as:

$$\Delta_1 = \frac{2 \times V_{in} \times D}{(V_b - V_{in})}, \tag{8}$$

#### 2.1.3 Third stage [$t_2$, $t_3$]

During this stage, both of the diodes $D_3$ and $D_4$ are OFF, $i_{L1}$ and $i_{L2}$ arrive at the freewheeling current $i_{fw}$, while $i_{fw}$ flows through $D_1$, $C_1$, $C_2$, $L_1$, $L_2$, and $D_{S2}$. This stage remains unchanged until the next turn-on of a new switching cycle.

Theoretical waveforms of the modified bridgeless SEPIC PFC converter are depicted in Fig. 4.

### 2.2 Full bridge buck converter

The main objective of the full bridge buck converter is to step down the output voltage of the modified bridgeless SEPIC PFC converter to a desired value. For each switching cycle, the switching pairs $S_3$–$S_6$ and $S_4$–$S_5$ are turned ON alternately (Fig. 1). There are four operation modes of the FB buck converter as illustrated in Fig. 5.

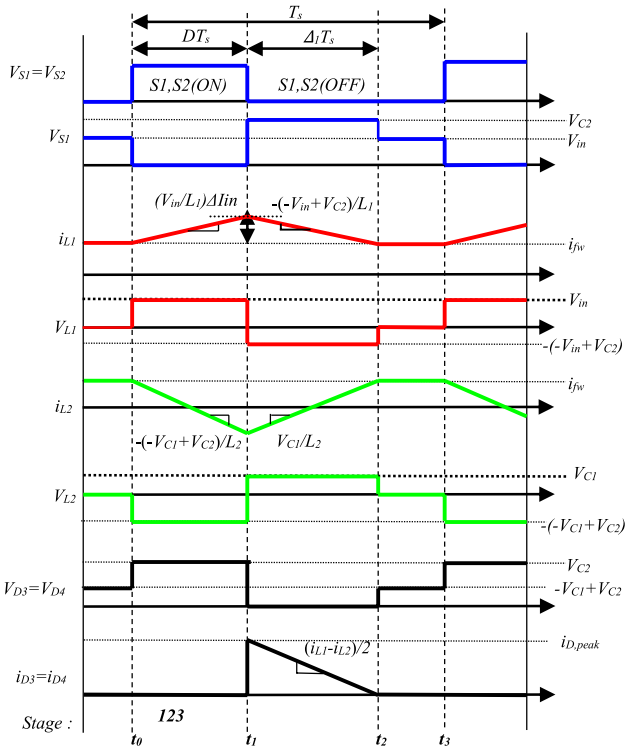


**Fig. 4** Waveforms of the modified bridgeless SEPIC converter [7]

#### 2.2.1 First stage

During this stage, the switches $S_3$ and $S_6$ are turned ON, while $S_4$ and $S_5$ are turned OFF as shown in Fig. 5a. The diode $D_{o1}$ becomes forward biased. The energy is stored in $L_o$, which increases the inductor current and discharges the capacitor $C_0$ through the output welding load.

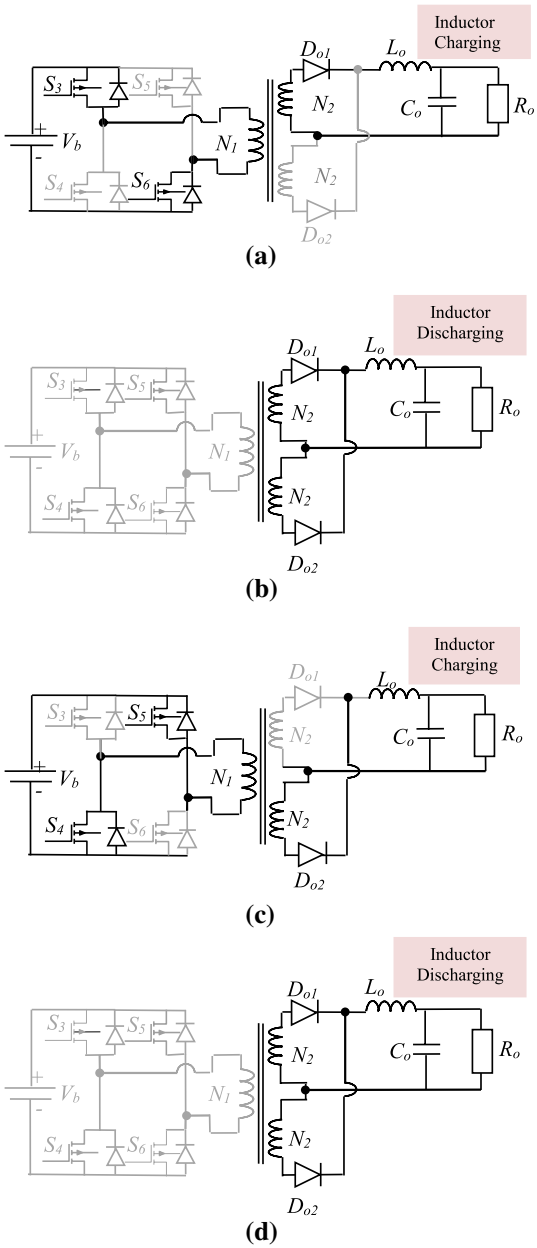


**Fig. 5** Operation modes of a full bridge buck converter: **a** stage 1. **b** stage 2. **c** stage 3. **d** stage 4

#### 2.2.2 Second stage

During this stage, as illustrated in Fig. 5b, all the switches are turned OFF, and $D_{o1}$ and $D_{o2}$ acts as the freewheeling diode. The output inductor discharges the energy to the capacitor $C_o$ and the output welding load.

#### 2.2.3 Third stage

Like the first stage, the switches $S_4$ and $S_5$ transfer energy to the inductor (Fig. 5c). The energy stored in $C_o$ is dissipated through the welding load.

#### 2.2.4 Fourth stage

This stage is similar to the second stage (Fig. 5d). $D_{o1}$ acts as the freewheeling diode. The energy stored in the inductor is used to charge the capacitor $C_o$. This stage ends up when the switches $S_3$ and $S_6$ are switched on again.

## 3 Circuit analysis

### 3.1 *Intermediate capacitor* $C_b$

The value of the capacitor $C_b$ depends on the voltage ripple $\Delta V_b$. Assuming that $\Delta V_b = 6\%$, the value of the intermediate capacitor $C_b$ can be calculated as [7]:

$$C_b = \frac{P_o}{4f\, V_b\, \Delta V_b} = \frac{2000}{4 \times 50 \times 400 \times 24} = 1041.66\ \mu F, \quad (9)$$

where $P_o$ is the input power, and the value of $C_b$ is chosen as 1100 µF.

### 3.2 *Input inductor* $L_1$

To guarantee the DCM operation, the following inequality must be satisfied:

$$D \langle \frac{V_b - V_{in\_eff} \times \sqrt{2}}{V_b + V_{in\_eff} \times \sqrt{2}} = \frac{400 - 220 \times \sqrt{2}}{400 + 220 \times \sqrt{2}} = 0.12, \quad (10)$$

The input inductor $L_1$ is selected so that the inductor current is approximately sinusoidal with an adequate ripple current of $\Delta i_{in} = 10\%$. The input current can be calculated as [7]:

$$i_{in} = \frac{2 \times Po}{\eta \times V_{in\_eff} \times \sqrt{2}} = \frac{2 \times 2000}{0.98 \times 220 \times \sqrt{2}} = 13.15\ \text{A}, \quad (11)$$

where $\eta$ is the efficiency of the converter.

The value of $L_1$ can be calculated as:

$$L_1 = \frac{V_{in\_eff} \times \sqrt{2} \times D}{\Delta i_{in} \times f_s} = \frac{220 \times \sqrt{2} \times 0.12}{1.31 \times 20000} = 1.42\ \text{mH}. \quad (12)$$

The value of $L_1$ is chosen as 1.5 mH.

### 3.3 *Output inductor* $L_2$

The output inductor $L_2$ can be calculated from $1/L_e = (1/L_1) + (1/L_2)$, where the value of $L_e$ is computed as follows [7]:

$$L_e = \frac{\left(V_{in\_eff} \times \sqrt{2}\right)^2 \times D^2}{2 \times \pi \times i_{in,\,avg} V_b \times f_s} \int_0^{\pi} \frac{\sin^2(\omega t)}{1 - \alpha \sin(\omega t)} d\omega t \quad (13)$$

$$\alpha = \frac{V_{in\_eff} \times \sqrt{2}}{V_b} = \frac{220 \times \sqrt{2}}{400} = 0.77 \quad (14)$$

### 3.4 *Output inductor* $L_o$

Assuming that $\Delta i_{L0} = 5\%$, the value of $L_o$ is calculated as:

$$L_0 = \frac{V_0 \times (0.5 - D_c)}{f_s \times \Delta i_{L0}} = \frac{20 \times (0.5 - 0.4)}{50000 \times 5} = 8\ \mu H, \quad (15)$$

where $D_c$ is the duty cycle for the rated output voltage $V_o$. It is expressed as:

$$D_c = \frac{V_0}{2 \times V_b} \times \left(\frac{N_1}{N_2}\right). \quad (16)$$

### 3.5 *Output capacitor* $C_o$

The voltage ripple $\Delta V_0$ is defined as [1]:

$$\Delta V_0 = \frac{V_0 \times (1 - 2 \times D_c)}{32 \times f_s^2 \times L_0 \times C_0}. \quad (17)$$

From Eq. (17), the value of $C_0$ is calculated as:

$$C_0 = \frac{V_0 \times (1 - 2 \times D_c)}{32 \times f_s^2 \times L_0 \times \Delta V_0} = \frac{20 \times (1 - 0.8)}{32 \times 50000^2 \times 8\ times 10^{-6} \times 2} = 3.12\ \mu F \quad (18)$$

The value of $C_0$ is chosen as 4 µF.

## 4 Proposed control scheme

The proposed control scheme is based on two controllers. (i) A PI controller for regulating the output voltage of the bridgeless modified SEPIC PFC converter. (ii) Another PI control scheme applied to the AWPS for DC voltage regulation.

### 4.1 Control of the modified bridgeless SEPIC PFC converter

The control of the modified bridgeless SEPIC converter is composed of two control loops. The first one is the voltage controller loop, which regulates the intermediate voltage ($V_b$) despite any changes in the parameters. The intermediate voltage is sensed and compared with its reference ($V_{bref}$), the obtained error ($e_{Vb}$) is processed by the PI controller as follows:

$$V_{cv}(k) = V_{cv}(k-1) + k_{pv}\left(e_{V_b}(k) - e_{V_b}(k-1)\right) + k_{iv}e_{V_b}(k), \tag{19}$$

where $k_{pv}$ and $k_{iv}$ are the proportional and integral gains of the PI controller, which were determined using the Ziegler and Nichols method.

The second one is the current control loop that uses the hysteresis control. The inductor current ($i_{L1}$) is sensed and compared with the reference ($i_{ref}$), where $i_{ref}$ is generated as the product of the output of the PI controller and the unit template of the supply voltage acting as a sinusoidal reference. The error between the reference current and the sensed current is processed by the hysteresis control (Fig. 6).

### 4.2 Control of a full bridge buck converter

The controller of a full bridge buck converter is intended to regulate the output voltage and to limit the output current. To fulfill the prerequisite of AWPS, two control loops are required. These loops are (1) the voltage loop used to regulate the dc output voltage, and (2) the current loop to restrict the output current during overload conditions.

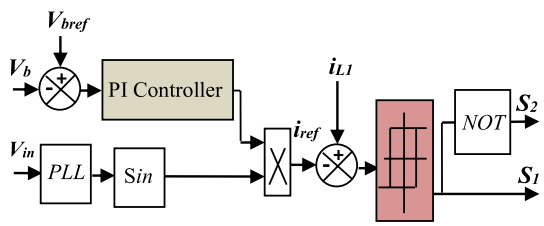


**Fig. 6** Block diagram of the control scheme for a modified bridgeless SEPIC PFC converter

The output voltage ($V_o$) is sensed and compared with its reference ($V_{oref}$), and the obtained error ($e_{Vo}$) is processed by the PI controller. The output of the PI controller is expressed as follows:

$$C_v(k) = C_v(k-1) + k_{pv}\left(e_{V_o}(k) - e_{V_o}(k-1)\right) + k_{iv}\,e_{V_0}(k), \tag{20}$$

where $k_{pv}$ and $k_{iv}$ are the proportional and integral gains of the PI, respectively.

The current controller constitutes a hysteresis controller where the output of the PI controller is compared with the sensed output current ($i_0$). The obtained error is processed by the hysteresis controller to generate the ON/OFF switching states (Fig. 7).

## 5 Results and discussion

The system under consideration is simulated in MATLAB/Simulink and implemented in real time for experimental validation using a HIL system based on a dSPACE DS1103 control board. The parameters of the system are given in Table 1.

### 5.1 Simulation

The system is simulated and evaluated for two cases: (1) AWPS under constant load conditions; and (2) AWPS under a load change.

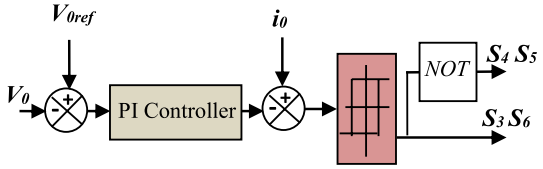


**Fig. 7** Block diagram of the control scheme for a FB buck converter

**Table 1** Specifications of the system under study

| Components | Symbol | Values |
|---|---|---|
| Input voltage | $V_{in}$ | 220 Vrms |
| Output DC voltage | $V_o$ | 20 V |
| Input inductors | $L_a$, $L_b$ | 1.5 mH |
| Input capacitors | $C_1$, $C_2$ | 0.047 µF |
| Intermediate capacitor | $C_b$ | 1100 µF |
| DC-link voltage | $V_b$ | 400 V |
| Output capacitor | $C_0$ | 4 µF |
| Output inductor | $L_0$ | 8 µH |

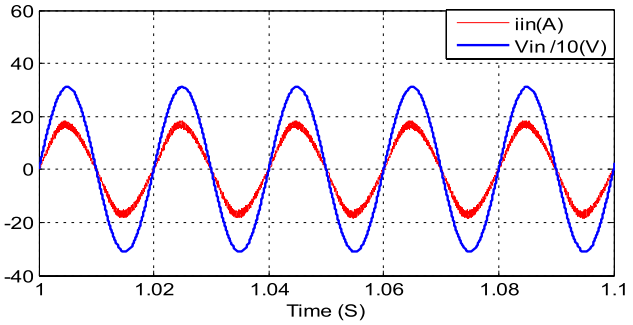


**Fig. 8** Input voltage and input current waveforms at the rated load

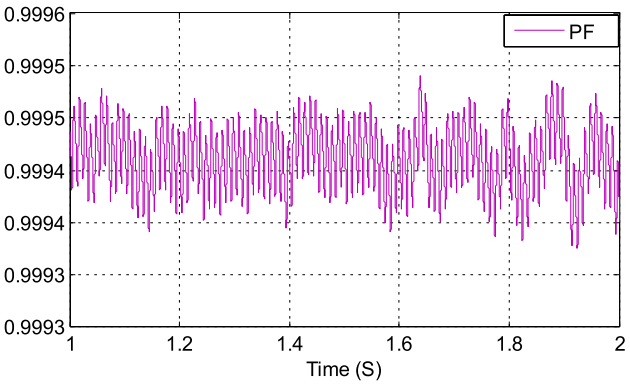


**Fig. 9** Measured PF at 220 V of AC grid

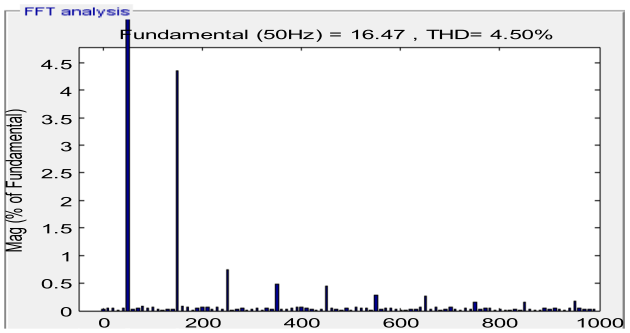


**Fig. 10** Measured THD at 220 V of AC grid

### 5.1.1 Case 1: AWPS under constant load conditions

Figures 8, 9, 10, 11, 12, 13 and 14 show the response of the AWPS at a constant load (0.2 Ω) with a fixed supply voltage ($V_{in}$) of 220 V (RMS), an output voltage ($V_o$) of 20 V and a ($V_b$) of 400 V. The input current ($i_{in}$) is in phase with the input voltage ($V_{in}$) (Fig. 8), which results in a unity PF (Fig. 9) and a low THD (Fig. 10). The peak voltage of the switches ($S_1$ and $S_2$) is around 750 V (Fig. 11), and the peak inductor current ($i_{L2}$) is 31 A (Fig. 12), which is sufficient

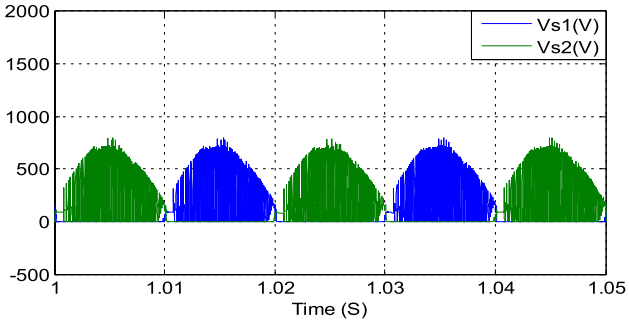


**Fig. 11** Voltages of switches ($V_{S1}$ and $V_{S2}$)

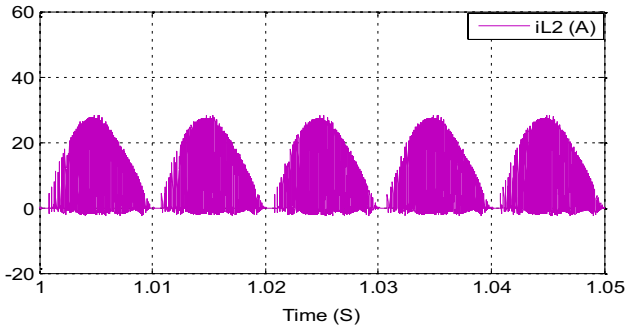


**Fig. 12** Inductor current ($i_{L2}$)

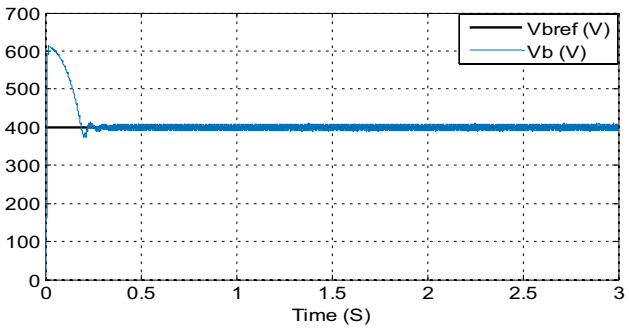


**Fig. 13** Intermediate capacitor voltage ($V_b$)

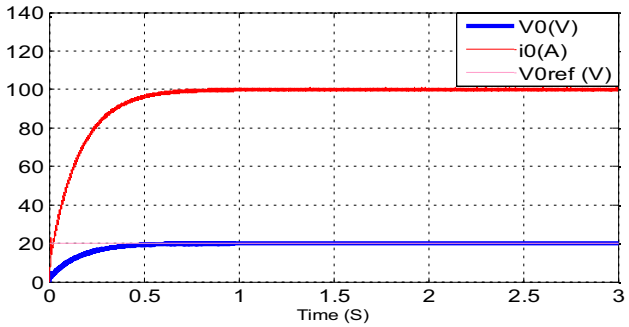


**Fig. 14** Output arc voltage ($V_o$) and welding load current ($i_o$)

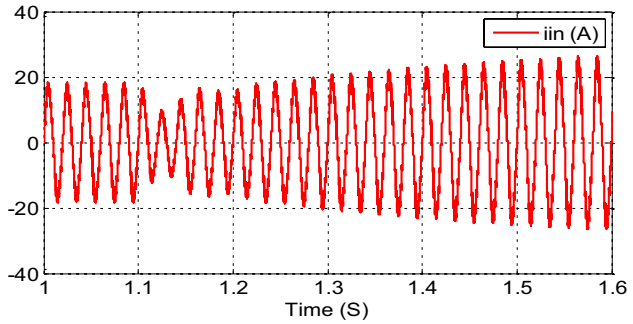


**Fig. 15** Waveform of the input current under a load change

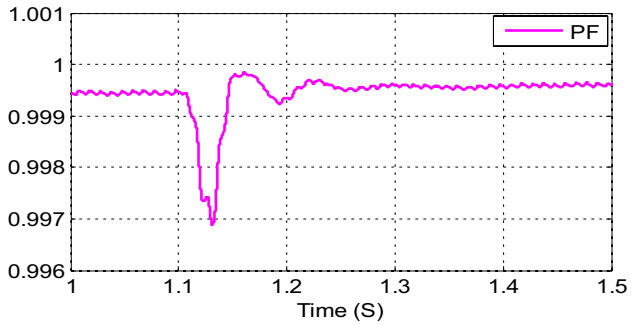


**Fig. 16** Measured PF under a load change

for operation in the DCM of the modified bridgeless PFC converter. The output voltage ($V_o$), welding current ($i_o$), and intermediate capacitor voltage ($V_b$) remain stable at their references without a steady state error and with a fast response time (Figs. 13, 14).

#### 5.1.2 Case 2: AWPS under a load change

The system is tested during a sudden load variation when the system is operating in the steady state. A step change is applied to the output load from 0.20 to 0.10 Ω with a fixed input voltage at 220 V (RMS) and an output voltage at 20 V. The obtained results are shown in Figs. 15, 16 and 17. It can be seen that the input current is in sinusoidal waveform (Fig. 15) with a unity PF (Fig. 16), and that the DC-link voltage is close to its reference (Fig. 17) with a small fluctuation leading a constant output current and a high-quality weld.

### 5.2 Impact of the load

The impact of load ($R_o$) variations based on various power quality (PQ) indices, such as PF and THD, are shown in Fig. 18. It is important to note that the PF is very close to unity, and that the THD at the AC mains current is < 5% at nominal line and load conditions.

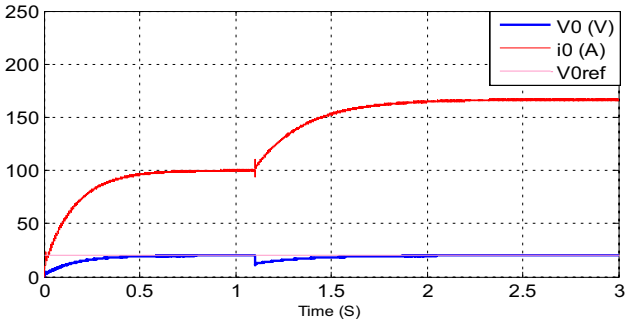


**Fig. 17** Output voltage and output current variation under a load change

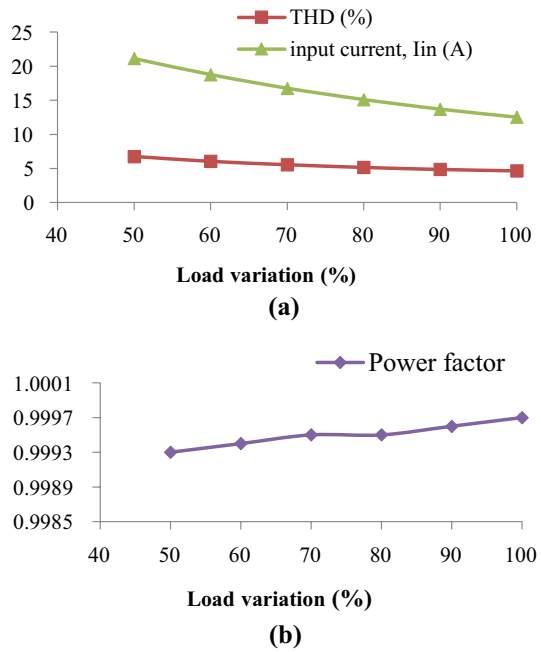


**Fig. 18** PQ indices of the bridgeless SEPIC PFC-based AWPS under welding load variations: **a** THD and input current. **b** PF

### 5.3 Comparative study

The performance of the modified bridgeless SEPIC PFC converter-based AWPS is compared with: (i) a traditional AWPS that contains a diode bridge rectifier followed by a full bridge buck circuit, and (ii) a boost PFC converter based AWPS for different values of input power, as shown in Fig. 19. From Fig. 19a, it is found that the PF obtained with the modified bridgeless SEPIC PFC based AWPS varies from 0.9993 to 0.9997. The PF achieved by the boost PFC converter based AWPS varies from 0.9 to 0.996. However, a very low PF (< 0.91) is achieved for the traditional AWPS. Moreover, the efficiency of AWPSs are compared as shown in Fig. 19b. It is evident that the modified bridgeless

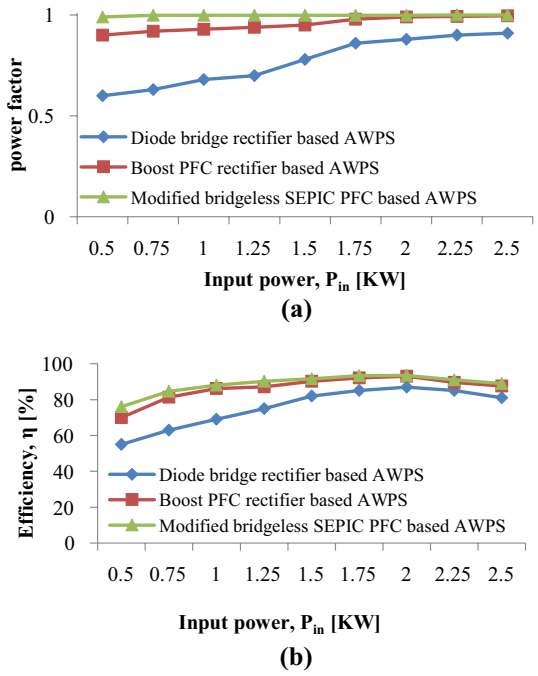


**Fig. 19** Comparative study in terms of: **a** power factor. **b** Efficiency for different values of input power

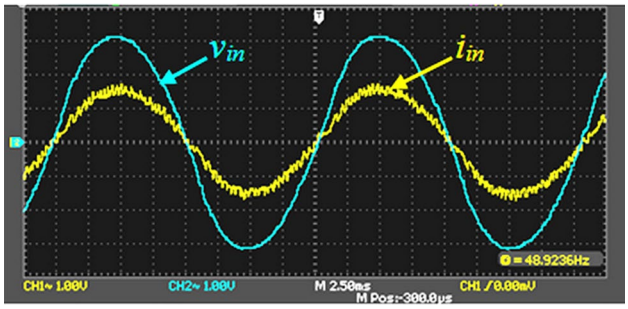


**Fig. 20** Experimental responses of the input voltage and input current

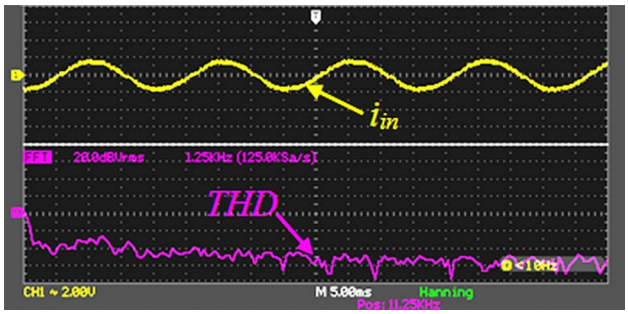


**Fig. 21** Experimental responses of the input current and THD

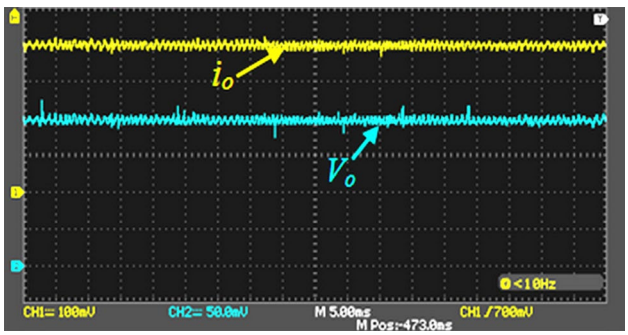


**Fig. 22** Experimental responses of the output voltage and output current

SEPIC PFC converter-based AWPS was able to guarantee a significant increase in efficiency (93.25%) when compared to the other configurations.

## 5.4 Experimental validation

A hardware in the loop (HIL) system based on a DS1103R&D controller board was used to implement and experimentally test the proposed control in real time, and to determine the computational limitations and the problems that can be found in experimental implementation.

The HIL involves the following steps:

1. Build a control system using the Simulink tool.
2. Generate different control results.
3. Download the program in C code to dSPACE using the Real-Time Workshop (RTW) tool.
4. Execute the overall plant model in real-time using the DS1103 card.

The performance of the AWPS is evaluated in the steady state. As shown in Fig. 20, the input current is in phase with the input voltage, which leads to a unity PF. The THD is well within acceptable limits (Fig. 21).

Figure 22 shows that the output voltage and welding output current are kept constant, which results in good arc stability. Figure 23 shows experimental responses of the inductor current ($i_{L2}$) and the intermediate capacitor voltage ($V_b$). As seen, there is accuracy accordance between the simulation and the experimental.

It can be observed from Fig. 24 that for a step changes in the load, (increasing by 50%) with fixed output voltage, the input current is in sinusoidal waveform, which leads to a unity PF. In addition, the proposed control scheme shows a high accuracy in terms of output voltage tracking regardless of load changes.

To test the proposed control under input voltage variations, a 15% increase of the mains voltage was applied to the system under study with fixed load at 0.2 Ω. It can be

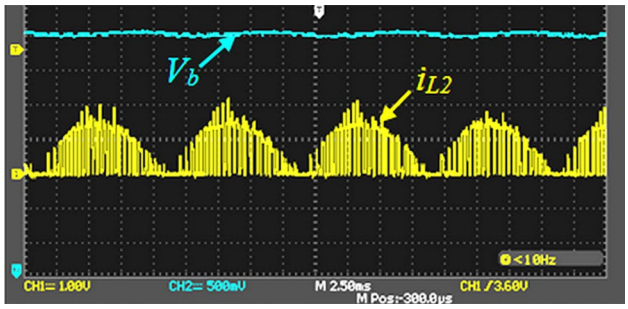


**Fig. 23** Experimental responses of the inductor current and intermediate capacitor voltage

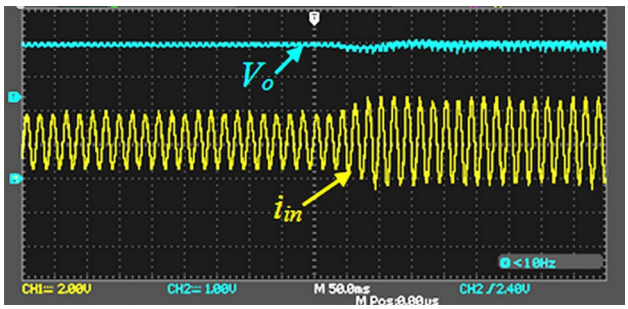


**Fig. 24** Experimental responses of the output voltage and input current during a step change of $R_0$ from 0.2 Ω to 0.1 Ω

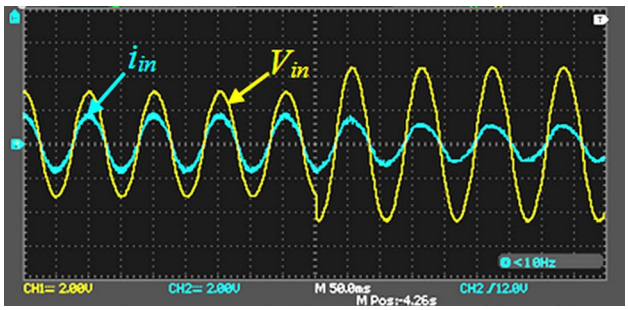


**Fig. 25** Experimental responses of the input voltage and input current when the mains voltage increases by 15%

seen from Fig. 25 that the input current is not affected by the voltage change, and that it is a sinusoidal waveform.

Figures 26 and 27 show waveforms of the input voltage and input current when the mains voltage contains 20% third harmonics component (Fig. 26), and 20% third harmonic and 10% fifth harmonics component (Fig. 27). Again, the suitable performance of the applied control can be clearly

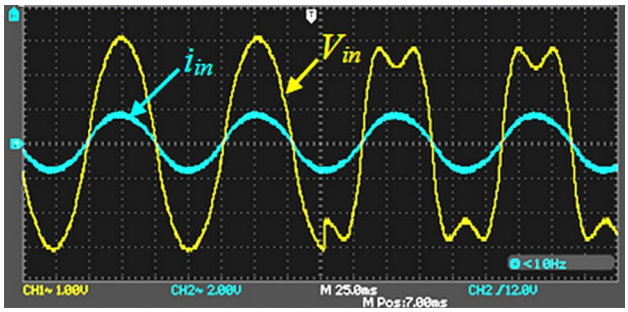


**Fig. 26** Experimental responses of the input voltage and input current when the mains voltage contains 20% third harmonic component

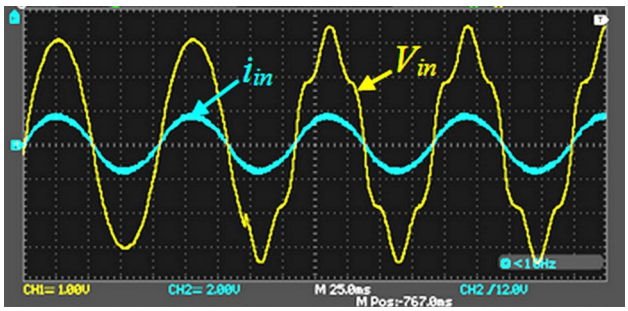


**Fig. 27** Experimental responses of the input voltage and input current when the mains voltage contains 20% third harmonic and 10% fifth harmonics components

observed, which achieves a sinusoidal input current, without harmonic content shown by the mains voltage.

## 6 Conclusions

This paper presented a new configuration and control scheme for an arc welding power supply. The configuration was based on a modified bridgeless SEPIC PFC converter. The good weld bead quality and unity PF were achieved with the control scheme developed for output voltage regulation. The system under study was tested by simulations and experiments in a HIL system. The obtained results demonstrate the accuracy accordance between the simulation and the experimental results. In fact, the input current was in the same phase as the input voltage. In addition, the THD of the AC grid met the international PQ standards and the PF was almost unity (0.999). This demonstrated that the AWPS was able to work with a high power quality. Furthermore, a good performance and a fast convergence were achieved under different load variations, which verify the effectiveness and the potential of the proposed approach.

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**Amar Bouafassa** was born in Sétif, Algeria, in 1988. He received his M.S. and Ph.D. degrees in Automatic Control from the University of Setif-1, Sétif, Algeria, in 2011 and 2015, respectively. He is presently working as a Lecturer at the National Polytechnic School of Constantine, Constantine, Algeria. His current research interests include modern control of power converters, PWM rectifiers, power factor correction, and energy efficiency.

**Luis M. Fernández-Ramírez** was born in Los Barrios, Cadiz, Spain. He received his M.S. degree in Electrical Engineering from the University of Seville, Seville, Spain, in 1997; and his Ph.D. degree in Industrial Engineering from the University of Cadiz, Cadiz, Spain, in 2004. From 1997 to 2000, he was with the Department of Development and Research, Desarrollos Eolicos SA, Seville, Spain. In 2000, he joined the University of Cadiz, where he is presently working as an Associate Professor in the Department of Electrical Engineering and as Head of the Research Group in Sustainable and Renewable Electrical Technologies (PAIDI-TEP023). His current research interests include smart grids, renewable energy sources, energy storage systems, hydrogen and fuel cell systems, electric vehicles, power converters, and energy management/control systems.

**Badreddine Babes** was born in El Eulma, Algeria, in 1980. He received his B.S., M.S., and Ph.D. degrees in Electrical Engineering from the University of Setif-1, Sétif, Algeria, in 2004, 2010, and 2018, respectively. Since 2017, he has been with the Research Center in Industrial Technologies (CRTI), Algiers, Algeria. His current research interests include predictive control of linear and nonlinear systems applied to motor drives and renewable energy systems, and pulse current control of gas metal arc welding (GMAW) processes.